## Claims

We claim:

1. A receiver, comprising:

a first means for receiving as inputs a first signal and a second signal;

a second means for generating as an output a third signal; and

a third means for adding delay to a propagation path of the first signal, said third means for adding being responsive to a first glitch on the third signal caused by the receiver sensing a first transition on the first signal before the receiver sensing a second transition on the second signal.

2. The receiver of claim 1, wherein the first transition is a rising transition and the delay affects only rising transitions of the first signal.

3. The receiver of claim 1, wherein the first transition is a falling transition and the delay affects only falling transitions of the first signal.

4. The receiver of claim 1, further comprising a fourth means for subtracting delay from a propagation path of the first signal, said fourth means being responsive to a second glitch on the third signal caused by the receiver sensing a third transition on the first signal after the receiver sensing a fourth transition on the second signal.

5. The receiver of claim 4, wherein the third transition is a rising transition and the delay affects

only rising transitions of the first signal.

6. The receiver of claim 4, wherein the third transition is a falling transition and the delay affects only falling transitions of the first signal.

7. A receiver for interpreting signals sent on a bi-directional, simultaneous transmission line, the receiver comprising:

a first comparator configured to receive into its positive and negative inputs a three-state digital signal from the transmission line and a first reference voltage level, respectively, and generate a first two-state digital signal, the three-state digital signal having first, second, and third state voltage levels, respectively;

a second comparator configured to receive into its positive and negative inputs the three-state digital signal from the transmission line and a second reference voltage level, respectively, and generate a second two-state digital signal; and

a logic circuit configured to receive as inputs the first and second two-state digital signals and a third two-state digital signal and to generate as an output a fourth two-state digital signal as a function of the first, second, and third two-state digital signals, wherein

the first reference voltage level is higher than the second reference voltage level, and

the first, second, and third state voltage levels are above the first reference voltage level, between the first and second reference voltage levels, and below the second reference voltage level, respectively.

8. The receiver of claim 7, further comprising:

a glitch detector electrically coupled to the logic circuit; and

a programmable delay unit electrically coupled to the glitch detector, wherein in response to a glitch on the fourth two-state digital signal, the glitch detector is configured to cause the programmable delay unit to adjust delay to a propagation path of the third two-state digital

signal.

9. The receiver of claim 8, wherein the glitch detector is further configured to receive as inputs the first, second, third, and fourth two-state digital signals and generate as an output a fifth control signal to the programmable delay unit, wherein the fifth control signal controls the adding of delay by the programmable delay unit to the propagation path of only rising transitions of the third two-state signal.

10. The receiver of claim 8, wherein the glitch detector is further configured to generate as an output a sixth control signal to the programmable delay unit, wherein the sixth control signal controls the adding of delay by the programmable delay unit to the propagation path of only falling transitions of the third two-state signal.

11. The receiver of claim 8, wherein the glitch detector is further configured to generate as an output a seventh control signal to the programmable delay unit, wherein the seventh control signal controls the subtracting of delay by the programmable delay unit from the propagation path of only rising transitions of the third two-state signal.

12. The receiver of claim 8, wherein the programmable delay unit comprises:

a capacitor; and

a first set of transistors in parallel and electrically coupled to the capacitor, wherein the programmable delay unit is configured to turn OFF at least one transistor of the first set of

transistors causing the capacitor to take longer to recharge/discharge resulting in the adding of delay by the programmable delay unit to the propagation path of only rising transitions of the third two-state signal.

13. The receiver of claim 12, further comprising a second set of transistors in parallel and electrically coupled to the capacitor, wherein the programmable delay unit is further configured to turn OFF at least one transistor of the second set of transistors causing the capacitor to take longer to recharge/discharge resulting in the adding of delay by the programmable delay unit to the propagation path of only falling transitions of the third two-state signal.

14. A method for interpreting signals sent on a bi-directional, simultaneous transmission line, the method comprising the steps of:

using a first comparator to receive into its positive and negative inputs a three-state digital signal from the transmission line and a first reference voltage level, respectively, and generate a first two-state digital signal, the three-state digital signal having first, second, and third state voltage levels, respectively;

using a second comparator to receive into its positive and negative inputs the three-state digital signal from the transmission line and a second reference voltage level, respectively, and to generate a second two-state digital signal; and

using a logic circuit to receive as inputs the first and second two-state digital signals and a third two-state digital signal and generate as an output a fourth two-state digital signal as a function of the first, second, and third two-state digital signals, wherein the first reference voltage level is higher than the second reference voltage level, and the first, second, and third state voltage levels are above the first reference voltage level, between the first and second reference voltage levels, and below the second reference voltage level, respectively.

15. The method of claim 14, further comprises the steps of:

providing a glitch detector electrically coupled to the logic circuit, and a programmable delay unit electrically coupled to the glitch detector; and

in response to a glitch on the fourth two-state digital signal, using the glitch detector to cause the programmable delay unit to adjust delay to a propagation path of the third two-state digital signal.

16. The method of claim 15, wherein the step of using the glitch detector to cause the programmable delay unit to adjust delay to a propagation path of the third two-state digital signal comprises the step of using the glitch detector to receive as inputs the first, second, third, and fourth two-state digital signals and generate as an output a fifth control signal to the programmable delay unit, wherein the fifth control signal controls the adding of delay by the programmable delay unit to the propagation path of only rising transitions of the third two-state signal.

17. The method of claim 15, wherein the step of using the glitch detector to cause the programmable delay unit to adjust delay to a propagation path of the third two-state digital signal comprises the step of using the glitch detector to generate as an output a sixth control signal to the programmable delay unit, wherein the sixth control signal controls the adding of delay by the programmable delay unit to the propagation path of only falling transitions of the third two-state signal.

18. The method of claim 15, wherein the step of using the glitch detector to cause the programmable delay unit to adjust delay to a propagation path of the third two-state digital signal comprises the step of using the glitch detector to generate as an output a seventh control signal to the programmable delay unit, wherein the seventh control signal controls the subtracting of delay by the programmable delay unit from the propagation path of only rising transitions of the third two-state signal.

19. The method of claim 15, further comprising the steps of:

providing a capacitor and a first set of transistors in parallel and electrically coupled to the capacitor; and

turning OFF at least one transistor of the first set of transistors causing the capacitor to take longer to recharge/discharge so as to perform the adding of delay by the programmable delay unit to the propagation path of only rising transitions of the third two-state signal.

20. The method of claim 19, further comprising the steps of:

providing a second set of transistors in parallel and electrically coupled to the capacitor; and

turning OFF at least one transistor of the second set of transistors causing the capacitor to take longer to recharge/discharge so as to perform the adding of delay by the programmable delay unit to the propagation path of only falling transitions of the third two-state signal.